

IN THE SPECIFICATION:

Please amend paragraph [0006] as follows:

[0006] With each new fabricating generation, the number of memory cells per die has historically increased by a factor of four. For example, what is commonly referred to as the 256K generation (262,144 addressable DRAM cells per chip) led to the 1M generation (1,048,576 addressable DRAM cells per chip). The 1M generation led next to the 4M generation (4,194,304 addressable DRAM cells per chip). The 4M generation led to the 16M generation (16,777,216 addressable DRAM cells per chip), which next led to the 64M generation (67,108,864 addressable DRAM cells per chip). The industry is presently working on the next factor of four generation, referred to as 256M (268,435,456 DRAM cells per chip), which has a memory cell pitch of 0.6 micron. Historically, with each generation, the number of addressable memory cells per chip increases exactly by a factor of four with an attendant increase in chip area. However, the increase in chip area has not been directly proportional to the increase in cells due to improved processing techniques which enable the individual memory cell size to be shrunk and thereby ~~density to increase in density~~. Nevertheless, each next generation puts four times the number of memory cells from the previous generation on a single chip.

Please amend paragraph [0045] as follows:

[0045] However, at the edges of the nitride, some oxidant also diffuses laterally. This causes the oxide to grow under and lift the nitride edges. Because the shape of the oxide at the nitride edges is that of a slowly tapering oxide wedge that merges into another previously formed layer of oxide, it has commonly been referred to as a "bird's beak." The bird's beak is a lateral extension or encroachment of the field oxide into the active areas where the devices are formed. Although the length of the bird's beak depends upon a number of parameters, the length is typically 0.15 ~~micron~~ 0.5- micron to 0.5 micron per side.

Please amend paragraph [0053] as follows:

[0053] The discussion initially proceeds with description of processes for forming field oxide regions in manners which minimize bird's beak encroachment into substrate active areas.

Fig. 1 illustrates a semiconductor wafer fragment in process for formation of a pair of adjacent field oxide regions having a minimum pitch of less than or equal to 0.7 micron, and is indicated generally with reference numeral 10. Such is comprised of a starting bulk semiconductor silicon substrate 12. A sacrificial pad oxide layer 14 is thermally grown over semiconductor silicon substrate 12 to a thickness of from 20 Angstroms to 100 Angstroms. A nitride masking layer 15, preferably Si_3N_4 , is provided over sacrificial pad oxide layer 14 to a thickness of from 500 Angstroms to 3000 Angstroms. The function of sacrificial pad oxide layer 14 is to cushion the transition of stresses between silicon substrate 12 and nitride masking layer 15. Nitride masking layer 15 will function as ~~the~~ a masking layer for ultimate formation of the field oxide regions.

Please amend paragraph [0054] as follows:

[0054] Referring to Fig. 2, nitride masking layer 15 has been patterned and etched as shown to form nitride masking blocks 16, 17 and 18. A channel-stop implant can be conducted prior to removing the illustrated nitride masking blocks. The etch to produce nitride masking blocks 16, 17 and 18 is substantially selective to sacrificial pad oxide layer 14. However, the etch does result in removal of a portion of sacrificial pad oxide layer 14 in an uneven manner due in part to the inherent preferred thinness of sacrificial pad oxide layer 14. Nitride masking blocks 16, 17 and 18 are provided to define and thereby overlie desired active area regions on the silicon substrate 12. The illustrated nitride masking blocks 16, 17, and 18 provide an example of a preferred minimum pitch 20 of adjacent blocks of less than or equal to 0.7 micron, with 0.6 micron being a specific example.

Please amend paragraph [0055] as follows:

[0055] Referring to Fig. 3, the wafer fragment 10 is preferably subjected to a wet isotropic etch to remove remaining portions of exposed sacrificial pad oxide layer 14 from the silicon substrate 12. This also produces undercut etching of sacrificial pad oxide layer 14 beneath nitride masking blocks 16, 17 and 18, as shown.

Please amend paragraph [0058] as follows:

[0058] Referring to Fig. 6, second masking layer 32 is anisotropically etched to define pairs 33, 34 and 31 of second masking layer sidewall spacers over silicon layer 30 and to outwardly expose portions of silicon layer 30. The anisotropic etch is preferably conducted selectively relative to silicon layer 30, as shown. Pairs 33, 34 and 31 of second masking layer sidewall spacers define interconnected respective pairs 35, 36 and 37 of respective masked laterally opposed and outwardly projecting foot portions of silicon layer 30.

Please amend paragraph [0060] as follows:

[0060] Referring to Fig. 8, second masking layer sidewall ~~spacers~~ spacer pairs 33, 34 and 31 are stripped from the silicon substrate 12. Alternately, these spacers can remain at this point in the process and be stripped after field oxidation. ~~Further~~ Further, as an alternative, ~~spacers~~ second masking layer sidewall spacer pairs 33, 34 and 31 might remain after field oxidation. Most preferred is removal of such spacers now as shown in Fig. 8.

Please amend paragraph [0061] as follows:

[0061] Referring to Fig. 9, the wafer is subjected to oxidizing conditions which oxidize the silicon of bulk silicon substrate 12 and silicon sidewall ~~spacers~~ spacer pairs 38, 40 and 42 to form the illustrated field oxide regions 44, 45. Any of a number of oxidizing conditions might be used. One example includes oxidizing in an O₂ ambient at a pressure of at least 15 atmospheres. The atmosphere will preferably be essentially void of H₂O during the oxidizing and constitutes essentially pure O₂ or O₂ injected into the reactor in combination with a carrier gas, such as N₂ or Ar. The preferred upper pressure limit for such an oxidation is 50 atmospheres, with 25 atmospheres being a more preferred condition. The preferred temperature range during such an oxidation is from 950°C to 1300°C. Growth rate in such a dry oxygen ambient at 25 atmospheres pressure at 1000°C is 4000 Angstroms per 70 minutes. Such oxidation is preferably conducted to provide field oxide regions 44 and 45 to have a location of maximum thickness of from 1500 Angstroms to 3000 Angstroms. As depicted, field oxide regions 44 and 45 define substrate active area 25 therebetween. During field oxidation, a very thin layer of oxide ~~(20—200~~

(20 to 200 Angstroms, not shown) may form atop nitride masking blocks 16, 17 and 18 from transformation of the Si_3N_4 to SiO_2 .

Please amend paragraph [0062] as follows:

[0062] Also during oxidation, silicon sidewall-~~spacers~~ spacer pairs 38, 40 and 42, being of a silicon material similar to silicon substrate 12, are also oxidized and grow in volume to approximately twice their original size. This results in formation of what is referred to as “Mickey Mouse” ears 46. However, the preferred 200 Angstroms to 1000 Angstrom thin nature of silicon layer 30, which ultimately forms silicon-~~spacers~~ sidewall spacer pairs 38, 40 and 42, results in smaller (thinner) “Mickey Mouse” ears 46. This provides the subsequent advantage of minimizing upper topography of the resultant field oxide regions 44 and 45. Further, the elongated nature of foot-~~portions~~ portion pairs 35, 36 and 37 (Fig. 8) advantageously provides adequate lateral displacement to prevent significant oxygen encroachment to minimize bird’s beak formation beneath nitride masking blocks 16, 17 and 18.

Please amend paragraph [0063] as follows:

[0063] Fig. 10 illustrates a diagrammatic top view of Fig. 9 emphasizing the illustrated field oxide regions 44 and 45, and active area 25 therebetween. A staggered layout of the active area regions is preferably utilized, with preferred minimum pitch 20 being the minimum pitch between the most closely adjacent field oxide regions 44 and 45. The staggering produces a wider pitch 21 (Fig. 10 only) between further spaced adjacent field oxide regions 44 and 45, as shown. During field oxidation, the location of maximum field oxide thickness typically occurs centrally relative to the respective widths of the regions along the wider pitch ~~line~~ 21. Field oxide thickness is typically less along preferred minimum pitch-~~line~~ 20, where substrate stress is greater due to closeness of the adjacent nitride masks.

Please amend paragraph [0064] as follows:

[0064] Fig. 11 illustrates stripping of nitride masking blocks 16, 17 and 18 from the silicon substrate 12, and subsequent stripping of second sacrificial oxide layer ~~material~~ 13.

Further, essentially any remnants of sacrificial pad oxide layer 14 which might be remaining would also be removed. In the course of such removals, any oxide formed atop nitride masking blocks 16, 17 and 18 would be removed, resulting in removal of oxide from atop field oxide regions 44 and 45 ~~in a~~ in quanta of from 50 Angstroms to 250 Angstroms. Further, removal of layer 13 will preferably remove an additional 50 Angstroms to 500 Angstroms of oxide from the field regions. Such also advantageously results in reduced ears 46a. Subsequently, a third sacrificial oxide layer 48 is preferably grown (i.e., from 150 Angstroms to 350 Angstroms over the silicon substrate) to eliminate the undesired formation of the silicon-nitride during the field oxidation (commonly referred to as the "Kooi effect"). Such oxide growth results in an estimated growth of field oxide regions 44 and 45 of from 50 Angstroms to 200 Angstroms.

Please amend paragraph [0065] as follows:

[0065] Referring to Fig. 12, third sacrificial oxide layer 48 is stripped from the silicon substrate 12. ~~Such 12, which~~ also etches from 200 Angstroms to 400 Angstroms of field oxide regions 44 and 45, and desirably has the effect of essentially eliminating the remaining sharp points of reduced ears 46a to produce an upper smooth topography for such field oxide regions. Thus, bird's beak encroachment into the active ~~area~~ area 25 is minimized. Field oxide regions 44 and 45 might also alternatively be provided to be recessed relative to bulk silicon substrate 12.

Please amend paragraph [0066] as follows:

[0066] The discussion next proceeds regarding improved techniques for roughening polysilicon surfaces for use in enhancing capacitance in capacitor constructions. More particularly and initially with reference to Figs. ~~13-15~~, 13 through 15, a semiconductor wafer fragment in process is indicated generally with reference numeral ~~50~~. ~~Such comprises 50, each comprising~~ a bulk semiconductor substrate 52 (typically p-doped monocrystalline silicon) having an n-type diffusion region 54 provided therein. Diffusion region 54 comprises a node to which electrical connection to a capacitor plate is to be made. A layer 56 of insulative silicon dioxide is provided over bulk semiconductor substrate 52 and is provided with a container opening 58

therein to diffusion region 54. The wafer is placed within a chemical vapor deposition reactor, and a layer 60 of *in situ* conductively doped amorphous silicon is chemical vapor deposited over the depicted substrate at a first temperature, which is below 600°C.

Please amend paragraph [0068] as follows:

[0068] Referring to Fig. 14, the substrate temperature within the reactor is raised at a selected rate to an annealing second temperature which is between 550°C and 950°C. The bulk semiconductor substrate 52 is maintained at the second annealing temperature for a period of time sufficient to convert doped amorphous silicon layer 60 into a doped polysilicon layer 65 having an outer surface 64 of a second degree of roughness which is greater than the first degree of roughness. ~~Substrate Bulk semiconductor substrate~~ 52 is not removed from the reactor nor exposed to any oxidizing conditions between the time of deposition of amorphous silicon layer 60 and its conversion to polysilicon layer 65.

Please amend paragraph [0069] as follows:

[0069] The selected ramp rate for the temperature increase is preferably less than or equal to 10°C/sec. Ramp rates of 30°C and 40°C were also utilized and while a roughness increase of outer surface 62 to outer surface 64 was observed, the increase was not as significant as where the ramp rate was kept at a lower rate of at or below 10°C/sec. The annealing second temperature is also kept at preferably below 700°C to minimize the thermal budget on the wafer during processing.

Please amend paragraph [0071] as follows:

[0071] Actual anneals were conducted at wafer temperatures of 650°C, 660°C, 670°C, 680°C, 700°C, 750°C, 800°C and 850°C. Reactor pressures were varied from 400 mTorr to 80 Torr with and without N₂. Deposition times ranged from 30 seconds to 900 seconds. Temperature ramp rates between the amorphous silicon deposition and the annealing ranged from 4°C/sec to 10°C/sec. The best results at producing maximized surface roughness of outer

surface 64 as compared to original outer surface 62 occurred at 670°C for between 30 and 60 seconds, where the ramp rate between deposition and anneal was approximately 5°C/sec.

Please amend paragraph [0073] as follows:

[0073] Figs. ~~16-18~~ 16 through 18 illustrate an alternate embodiment construction and process which incorporate at least one additional process step over that depicted by Figs. ~~13-15~~ 13 through 15. Like numbers from the embodiment of Figs. ~~13-15~~ 13 through 15 are utilized where appropriate, with differences being indicated with the suffix "a" or with different numerals. Fig. 16 illustrates the same essential Fig. ~~13~~ wafer fragment 50a incorporating additional features and at a processing step subsequent to that shown by Fig. 13. Specifically, and after provision of *in situ* doped amorphous silicon layer 60, the substrate temperature is raised at a selected rate to an intermediate silicon seeding temperature. At the seeding temperature, a discontinuous layer of silicon particles 69 is provided atop doped amorphous silicon layer 60. This occurs within the same reactor and without any intervening exposure of the wafer to oxidizing conditions between the time of amorphous silicon deposition and provision of the discontinuous seeding particles. The seeds constitute discrete clusters of silicon atoms.

Please amend paragraph [0075] as follows:

[0075] Referring to Fig. 17, the bulk semiconductor substrate 52, again within the same chemical vapor deposition reaction and without any intervening exposure of the wafer to oxidizing conditions, has its temperature raised at a ~~second~~ second selected rate to the annealing temperature, which is between 550°C and 950°C. Again, the preferred rate is at or below 10°C/sec. The substrate is maintained at the annealing temperature for a period of time sufficient to convert the doped amorphous layer into a doped polysilicon layer 65a having outer surface 64a, with such outer surface having a second degree of roughness which is greater than the first degree of roughness of amorphous silicon layer outer surface 62a.

Please amend paragraph [0076] as follows:

[0076] An advantageous phenomenon occurs in utilization of silicon particles 69. The amorphous silicon of layer 60 migrates on outer surface 62a and agglomerates onto the silicon seeds/particles 69, creating bumps and valleys and therefore an outer polysilicon surface having even greater roughness. Fig. 17 depicts the silicon particles 69 as being discrete at the conclusion to the annealing processing step. More typically, such particles would no longer exist as discrete particles and would rather constitute a part of the homogeneously formed polysilicon crystal lattice of doped polysilicon layer 65a. An exemplary annealing temperature wherein a silicon seeding temperature of 600°C is utilized would be 630°C. Also possible in accordance with the invention, the annealing temperature and seeding temperature might be the same temperature, such that the second selected temperature ramp rate is 0°C/sec.

Please amend paragraph [0082] as follows:

[0082] Such extra spacing can be overcome to a degree in a manner described with reference to Figs. 21-23. Like numerals from the embodiment of Figs. 19 and 20 are utilized where appropriate, with differences being indicated by the suffix “b” or with different numerals. Specifically, the lateral or horizontal misalignment tolerance between the respective container openings 76 and the adjacent mask opening outline 84 are reduced on each side of bit contact 86 opening ~~86~~ by a factor of the “y” spacing. Thus, in connection with the described embodiment, the adjacent pair of container openings 76 can be placed 0.3 micron closer to one another, thus increasing circuit density. Such is essentially accommodated for by allowing or providing for the misalignment tolerance of spacing “y” to be in a vertical direction as opposed to a horizontal direction.

Please amend paragraph [0085] as follows:

[0085] An example of integration of one or more of the above processes is described with reference to Figs. 24 and 25. Such illustrates a ~~semiconductive~~ semiconductor wafer fragment 90 comprised of a bulk substrate 92 and field oxide regions 94. Preferably, field oxide regions 94 are produced in accordance with the above-described processes to minimize bird's

beak encroachment. The area between field oxide regions 94 constitutes active area 95. A series of four word lines 96, 97, 98 and 99 are illustrated in Fig. 24. Each is comprised of a composite of five layers, namely, a gate oxide layer, a conductively doped polysilicon layer, a WSi_x layer, an oxide layer, and an Si_3N_4 capping layer. Electrically insulative sidewall spacers, typically formed of Si_3N_4 , are also provided relative to the respective word lines, as shown.

Please amend paragraph [0088] as follows:

[0088] An insulating dielectric layer 116, typically BPSG, is provided outwardly of capacitor constructions 102 and 104. Bit contact plug 106 provided therethrough and through insulating dielectric layer 100 to contact 108. Bit contact plug 106 preferably comprises the illustrated composite of layer 118 of titanium, layer 120 of TiN as a barrier layer, and layer 122 of elemental tungsten. Where layer 118 interfaces with bulk ~~silicon~~-substrate 92, a conductive WSi_x forms.

Please amend paragraph [0090] as follows:

[0090] Another insulating dielectric layer 132 is provided outwardly of ~~bit digit~~ line 124 and is provided with a planarized outer surface. Composite-patterned electrically conductive runners 136 are shown outwardly of insulating dielectric layer 132 (Fig. 24). Such conductive runners typically are not utilized as part of the DRAM memory array, but are utilized in the pitch and the peripheral circuitry of such arrays.

Please amend paragraph [0091] as follows:

[0091] Fig. 25 illustrates, by dashed ~~outline 140~~, outline, the area ~~which~~ that is consumed by a single memory cell in accordance with this embodiment. Such area can be considered or described as relative to a minimum capable photolithographic feature dimension "F." As shown, a single memory area 140 is 4F wide by 2F deep, thus providing a consumed area for a single memory cell of $8F^2$.

Please amend paragraph [0094] as follows:

[0094] This disclosure further provides an alternative process which enables elimination of field oxide regions within the memory array, thus facilitating greater circuit density. As background, field oxide regions provide electrical isolation between certain adjacent banks of memory cells within the array. Field oxide by definition defines breaks in the active area formed within the bulk substrate between adjacent cells. For example, see Fig. 25, which shows a break between the two adjacent active areas 95. Such results from field oxide formed therebetween, with the illustrated word lines ~~99 and 96~~ 96 and 99 running atop such field oxide region for gating a staggered set of memory cells within the array. The lateral expanse of the field oxide and word lines 96 and 99 for the staggered active area array constitute circuit area which is consumed on a semiconductor substrate. Specifically, each memory cell of a DRAM array has 1.5 times the minimum photolithographic feature size, F , of its lateral expanse consumed by field oxide and the area for word lines 96 and 99. In accordance with one preferred aspect of this disclosure, memory cell area devoted to electrical isolation from an adjacent cell and to word lines 96 and 99 can be reduced from $1.5F$ to $0.5F$.

Please amend paragraph [0095] as follows:

[0095] Specifically, Fig. 26 illustrates a continuous active area 295 formed within the bulk substrate relative to the associated overlying bit line 224. A series of capacitor contacts 207 and a series of bit line contacts 208 are formed relative to continuous active area 295. Word line pairs 297 and 298 share an intervening bit contact of adjacent pairs of memory cells, which in turn share a diffusion region in the bulk substrate. Electrical isolation between the adjacent pairs of memory cells is provided by intervening isolating conductive lines 225 which are formed in conjunction with the formation of word lines ~~line pairs~~ 297 and 298. Conductive lines 225 in operation are connected with ground or a suitable negative voltage, such as V_{ss} or V_{BB} , and effectively substitute for the electrical isolation formerly provided by field oxide.

Please amend paragraph [00100] as follows:

[00100] For example, Fig. 27 illustrates one embodiment of a vertical three-level twist or swap design of D and D* to facilitate achieving preferred equal bit line lengths running on the upper and lower levels of the design. As illustrated on the left side of Fig. 27, a digit ~~D line~~ line D₃₁₀ is on Level 1, while a complementary digit ~~line~~ D* line D*₃₁₂ is on a Level 2 and directly beneath D line 310. D line 310 drops down to Level 2 at 314, then to a Level 3 where it is routed around the D* line by a conductive area 316, and is then elevated back up to Level 2 at 315. Accordingly, D line 310 has achieved a twist or a swap in the vertical direction, or Z-axis, from Level 1 to Level 2. A similar vertical twisting or swapping occurs for complementary digit line D* ~~line~~ 312. It drops down from Level 2 to Level 3, is routed around D line 310 and conductive area 316 by a conductive area 318, and is then elevated to Level 2 at 313 and ultimately to Level 1 at 322. Accordingly, the twisting or swapping is relatively to the “z” direction, with attendant “x” and “y” areas being consumed on Level 3 for conductive areas 316 and 318.

Please amend paragraph [00101] as follows:

[00101] Fig. 28 shows an alternate four-level twist or swapping configuration. A conductive path 319 is provided at a sublevel 4. Sublevel 4 might comprise a substrate implant, polysilicon, metal, etc. Formation of a transistor from ~~conductive areas~~ area 316 and conductive path 319 is, however, highly undesirable.

Please amend paragraph [00102] as follows:

[00102] Fig. 29 shows an alternate three-level configuration. As shown, the twisting or swapping of D line 310 and complementary digit line D* ~~line~~ 312 occurs relative to Level 2 and Level 3 within Level 1.

Please amend paragraph [00103] as follows:

[00103] Fig. 30 shows another alternate configuration. Digit line D₃₃₀ is moved down one level to 336 via conductive areas 332 and 334, while D* is twisted upward to 340 via region 342. Region 342 extends outward in the x-y plane, while digit line D ~~line~~ 330/region 336

~~stays~~ stay in the same x-y configuration. Region 342 also extends into or within the vertical plane of an adjacent pair of digit lines D 346 and D* 348. To accommodate this extension of region 342, the bottom digit line D* line 348 is moved to Level 3 along a region 350 and then brought back up to Level 2.

Please amend paragraph [00105] as follows:

[00105] For ease of illustration in Fig. 31, the digit line pairs feeding the respective shared sense-amps- amplifier 370 appear as if they were horizontally spaced side-by-side relative to one another. In actuality, the subject digit line pairs are vertically oriented relative to one another in accordance with the above-described preferred embodiments. For example, with respect to the top pair illustrated in Fig. 31, a digit line D line 360 and a digit line D* line 364 are illustrated. Twisting or swapping relative to a vertical plane is indicated by the “x” crossing at location 368. Other staggered swapping of the other pairs ~~are~~ is also shown. Most desirably, each line of each pair spends 50% of its length on each of the top and bottom portion of the vertically aligned orientation.

Please amend paragraph [00106] as follows:

[00106] Referring to Fig. 32, a layout for a portion of a DRAM array having the preferred double-layer twisted digit lines is depicted. Six digit line pairs (DP0, DP1, DP2, DP3, DP4 and DP5) are shown in this abbreviated layout. Each pair consists of a D line and D* line aligned in a common vertical plane. The uppermost digit lines and lowermost digit lines are depicted as being of different widths for clarity in the drawings. In reality, they would be of the same width. The illustrated dashed rectangles comprise active areas, with ~~numerals~~ numeral 381 denoting bit contacts thereto. Lines 382 comprise word lines, while lines 383 are isolation lines substituting for field oxide as described above. Vertical contact vias (CV) are represented by the squares marked with an “X.”

Please amend paragraph [00115] as follows:

[00115] ~~Die Semiconductor die~~ 150 (Fig. 35) is comprised of a series of 64 multiple memory arrays 160 arranged as shown. The area immediately surrounding the respective ~~array areas-~~ memory arrays 160, such as the illustrated areas 162, contain what is referred to as pitch circuitry, as such circuitry is “on pitch” with the conductive lines which extend outwardly from the associated memory arrays 160. Such pitch circuitry 162 would comprise, for example, sense amplifier circuitry, equilibration circuitry, bias devices, I/O decoders, and other circuitry.

Please amend paragraph [00116] as follows:

[00116] Die areas ~~or regions~~ 164, 166, 168, 170, 172 and 174 constitute what is referred to as peripheral circuitry. Pitch circuitry areas 162 electrically connect with the peripheral circuitry areas, with the peripheral circuitry electrically interconnecting with the illustrated series of bond and probe pads 175. Suitable wires or other means would be utilized to connect with bond pads 175 to provide electrical connection to pins 156 of Fig. 34. The peripheral circuitry would preferably include the operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry, which collectively enable full access to all addressable memory cells of the memory arrays. For example, peripheral circuitry region 164 would typically comprise global column decode and column addressing circuitry. ~~-Section-~~ Region 174 could include section logic, DC sense amps and write drivers. Peripheral circuitry regions 170 and 172 would include power amplifiers, power busing and chip capacitors. Regions 166 and 168 would include other logic circuitry.

Please amend paragraph [00117] as follows:

[00117] One or more of the above-described processes and die configuration can facilitate formation of 64M, 16M, and 4M memory dice or devices having smaller sizes or consumed monolithic die areas than has heretofore been practically achieved. For example, at a 64M memory cell integration level, a total of no more than 68,000,000 ~~(typically-~~ typically, exactly 67,108,864) functional and operably addressable memory cells are arranged within collective multiple memory arrays 160. The occupied area of all of the functional and operably

addressable memory cells on the die consumed within the multiple memory arrays will have a total combined area which is no greater than 53 mm^2 .

Please amend paragraph [00118] as follows:

[00118] In accordance with standard semiconductor memory fabrication, the respective memory arrays are provided with redundant memory cells which, after test, can be operably fused to replace inoperable memory cells created during fabrication. Where an inoperable memory cell is determined during tests, the entire respective row (word line) or column (bit line) is fused out of operation, and an operable redundant row or ~~column~~ column is substituted in its place. Accordingly, during fabrication, the individual respective memory arrays, such as those shown in the above Fig. 35 example and for 16M integration, are intended to be fabricated to include more than 1/64th of the total operable memory cells of the finished memory device to contend with inoperable circuitry undesirably fabricated within the arrays.

Please amend paragraph [00119] as follows:

[00119] However, upon final fabrication and assembly, the respective memory arrays are provided to contain 1/64th of the total memory cells of the memory device/chip. Accordingly, each memory array 160 would have an area which is greater than the sum of 1/64th of the area which would be taken up by the total functional and operably addressable memory cells within the respective subarray. Regardless, that surface area of the die which is consumed by the memory cells which are finally functional and operably addressable through final fusing or other means will have a total combined area (although perhaps disjointed if internal inoperable cells are fused out) in this inventive example which is no greater than 53 mm^2 . However, the area consumed by a respective individual memory array 160 will be greater than 1/64th of the described 53 mm^2 due to the redundant circuitry. Sixty-four (64) subarrays are the preferred number for 16M integration, while 256 subarrays would be more preferred and typical for 64M integration.

Please amend paragraph [00120] as follows:

[00120] There will be areas on semiconductor die 150 within at least one memory array 160 where at least ~~100-square~~ 100-square microns of continuous die surface area has a collection of all operable memory cells, with no inoperable memory cells being included within that particular ~~100-square~~ 100-square micron area. In accordance with one aspect of the invention, there will be at least 128 memory cells within such ~~100-square~~ 100-square microns of continuous die surface area.

Please amend paragraph [00123] as follows:

[00123] Further, for the exemplary five composite conductive line layer construction, there will be areas on semiconductor die 150 within at least one memory array 160 where at least ~~100-square~~ 100-square microns of continuous die surface area have a collection of all operable memory cells, with no inoperable memory cells being included within that particular ~~100-square~~ 100-square micron area. In accordance with an aspect of the invention, there will be at least 170 memory cells within such ~~100-square~~ 100-square microns of continuous die surface area.

Please amend paragraph [00124] as follows:

[00124] In accordance with another aspect of the invention and at the 16M memory cell integration level, a total of no more than 17,000,000 (~~typically~~ typically, exactly 16,777,216) functional and operably addressable memory cells are provided by the multiple memory arrays 160. The occupied area of all of the functional and operably addressable memory cells on the die consumed within the multiple memory arrays will have a total combined area which is no greater than 14 mm^2 . Such is achievable, by way of example only and not by way of limitation, in the context of a four or less composite conductive line layer construction as described above with respect to Figs. 24 and 25. In such instance, the periphery circuitry, the pitch circuitry and the memory arrays have a total combined continuous surface area on the die which is less than or equal to 35 mm^2 . Also, at least one of the memory arrays which contains at least ~~100-square~~ 100-square microns of continuous die surface area will have at least 128 functional and operably addressable memory cells.

Please amend paragraph [00125] as follows:

[00125] Where five composite conductive line layers are utilized, the die area consumed by all of the functional and operably addressable memory cells will have a reduced total combined area (although again, most likely noncontinuous/disjointed) which is no greater than 11 mm^2 for 16M integration. Further, in such instance, the peripheral circuitry, the pitch circuitry and the memory arrays will have a total combined continuous surface area on the die which is less than or equal to 32 mm^2 . Further, at least one of the memory arrays which contain at least ~~100 square~~ 100-square microns of continuous die surface area will have at least 170 functional and operably addressable memory cells.

Please amend paragraph [00126] as follows:

[00126] For example, with respect to the above-described Fig. 35 depiction and a five composite conductive line layer construction, at the 16M integration level, each of the 64 memory arrays 160 would include 256K (truly 262,144) functional and operably addressable memory cells. An example of the ultimate dimension for semiconductor die 150 is 3.78 mm by 8.20 mm, resulting in a total continuous die area of 31.0 mm^2 .

Please amend paragraph [00127] as follows:

[00127] In accordance with another aspect of the invention and at the 4M memory cell integration level, a total of no more than 4,500,000 (~~typically~~ (typically, exactly 4,194,394) functional and operably addressable memory cells are provided by the multiple memory arrays 160. The occupied area of all of the functional and operably addressable memory cells on the die consumed within the multiple memory arrays will have a total combined area which is no greater than 3.3 mm^2 . Such is achievable, by way of example only and not by way of limitation, in the context of a four or less composite conductive line layer construction as described above with respect to Figs. 24 and 25. In such instance, the periphery circuitry, the pitch circuitry and the memory arrays have a total combined continuous surface area on the die which is less than or equal to 11 mm^2 . Also, at least one of the memory arrays which contain at least ~~100 square~~

~~100-square~~ microns of continuous die surface area will have at least 128 functional and operably addressable memory cells.

Please amend paragraph **[00128]** as follows:

[00128] Where five composite conductive line layers are utilized, the die area consumed by all of the functional and operably addressable memory cells will have a reduced total combined area (although again, most likely noncontinuous/disjointed) which is no greater than 2.5 mm^2 for 4M integration. Further, in such instance, the peripheral circuitry, the pitch circuitry and the memory arrays will have a total combined continuous surface area on the die which is less than or equal to 10.2 mm^2 . Further, at least one of the memory arrays which contain at least ~~100-square~~ ~~100-square~~ microns of continuous die surface area will have at least 170 functional and operably addressable memory cells.